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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/470,875	12/22/1999	MANPREET S. KHAIRA	2207/6843	6722

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EXAMINER	
CRAIG, DWIN M	

ART UNIT	PAPER NUMBER
2123	15

DATE MAILED: 08/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/470,875	KHAIRA ET AL.	
	Examiner	Art Unit	
	Dwin M Craig	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6-29-2004* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 7-56* is/are pending in the application.

4a) Of the above claim(s) *8* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5, 7 and 9-51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-5 and 7-55 have been presented for reconsideration in light of Applicant's Request for Reconsideration under 37 C.F.R. 1.114. Claim 8 has been cancelled as per Applicant's request.

Response to Arguments

2. Applicant's arguments filed on 6-29-04 have been fully considered. Examiners response is as follows:

2.1 Regarding Applicant's response to the 35 U.S.C. 103 rejections of Claims 1, 2, 4, 5, 8-10, 21, 22, 24-27, 29, 30, 31, 32, 34-43, 45, 46 and 48-55:

The Applicant has argued that:

...extraneous limitations were inadvertently included in the listings of claims 1, 21, 26, 29, 45, 51, 52, 54 and 55 that Applicants did not intend to include or argue.

And

No new matter has been added and no new search is required.

And

Claims 56 has been added to claim the same subject matter of inadvertently cancelled claim 8.

The Examiner has found no persuasive arguments, in regards to the current art rejections, that provide for allowance of Applicant's amended claims. The Examiner notes that by, *Applicant's Own Admission,* no new matter has been presented for Examination and no new arguments have been presented for re-consideration of the Examiner's prior art rejections. The Examiner has modified the original 35 U.S.C. 103(a) rejections of Applicant's claims to reflect the reshuffled disposition of the original claimed limitations.

Claim Rejections - 35 USC § 103

The Examiner has followed the factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, 4, 5, 7-10, 13-18, 21, 22, 24-27, 29, 30, 31, 32, 34-43, 45, 46, 48-51, and 53-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Eisenhofer et al. U.S. Patent 6,108,494** hereafter referred to as the *Eisenhofer–1* reference in view of **Worthington et al. U.S. Patent 5,881,270** and in further view of **Eisenhofer et al. U.S. Patent 6,339,836** hereafter referred to as the *Eisenhofer-2* reference.

3.1 As regards independent **Claims 1, 21, 26, 29, 34 and 51** the *Eisenhofer-1* reference discloses a method for distributed simulation **(Col. 7 Lines 15-25),** at least two simulators **(Figure 2),** a back plane **(Figure 2 Item 210),** an interface for the simulators **(Col. 5 Lines 52-67, Col. 6 Lines 1-20),** fixed configuration back plane **(Col. 5 Lines 5-7),** exchanging

messages **(Col. 8 Lines 42-47)** and data format conversions **(Col. 5 Lines 52-67, Col. 6 Lines 1-20, Col. 12 Lines 34-67, Col. 13 Lines 1-5).**

The *Eisenhofer-1* reference does not expressly disclose simulators that represent components of a system based on a processor and a chipset.

The *Worthington et al.* reference discloses a method for flexible simulation modeling that represent at least one of a component and a system based on processors and chipsets **(Figures 1, 3, 3A, 4, Col. 4 Lines 47-61).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have modified the *Eisenhofer-1* reference with the *Worthington et al.* reference because by providing entire multi-chip system models using individual system component models, an entire set of integrated circuits may be tested and simulated, not just individually, but in a manner that simulates how they will interact with each other such that problems in how the different chips interact can be detected before costly fabrication occurs ***(Worthington et al. Col. 1 Lines 45-51).***

3.2 As regards the limitation of an apparatus in independent **Claims 40 and 45** the *Eisenhofer-1* reference discloses an apparatus **(Figure 3, Col. 6 Lines 46-67, Col. 7 Lines 1-25).**

3.3 As regards independent **Claims 53-55** the *Eisenhofer-1* reference discloses an articled with a storage medium wherein there is stored instructions for a processor **(Figure 3, Col. 6 Lines 46-67, Col. 7 Lines 1-25).**

3.4 As regards the limitation of validating a component/ element of a design in independent **Claims 29, 34, 40 and 45** the *Eisenhofer-1* reference does not expressly disclose validation.

The *Worthington et al.* reference discloses validation **(Col. 8 Lines 30-40).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have modified the *Eisenhofer-1* reference with the *Worthington et al.* reference because by providing entire multi-chip system models using individual system component models, an entire set of integrated circuits may be tested and simulated, not just individually, but in a manner that simulates how they will interact with each other such that problems in how the different chips interact can be detected before costly fabrication occurs ***(Worthington et al. Col. 1 Lines 45-51).***

3.5 As regards **Claims 2, 22, 31, 38, 42 and 49** the *Eisenhofer-1* reference does not expressly disclose a driver.

The *Worthington et al.* reference discloses a driver **(Figure 1 Item 14b).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have modified the *Eisenhofer-1* reference with the *Worthington et al.* reference because by providing entire multi-chip system models using individual system component models, an entire set of integrated circuits may be tested and simulated, not just individually, but in a manner that simulates how they will interact with each other such that problems in how the different chips interact can be detected before costly fabrication occurs ***(Worthington et al. Col. 1 Lines 45-51).***

3.6 As regards **Claims 4, 24, 32, 39, 43, 50,** the *Eisenhofer-1* reference does not expressly disclose generating specific circuit models, however the reference does discuss the use of models in circuit simulation.

The *Worthington et al.* reference discloses models of components used in circuit simulation **(Figures 1-10, Col. 2 Lines 30-67, Col. 3 Lines 1-8).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have modified the *Eisenhofer-1* reference with the *Worthington et al.* reference because by providing entire multi-chip system models using individual system component models, an entire set of integrated circuits may be tested and simulated, not just individually, but in a manner that simulates how they will interact with each other such that problems in how the different chips interact can be detected before costly fabrication occurs ***(Worthington et al. Col. 1 Lines 45-51).***

3.7 As regards **Claims 5, 25, 27, 30, 35, 41 and 46** the *Eisenhofer-1* reference discloses an integrated circuit **(Col. 1 Lines 30-48).**

3.8 As regards **Claims 8, 9 and 56** the *Eisenhofer-1* reference discloses a global signal used for synchronization and simulators being relaxed based on the current state of that simulator **(Col. 6 Lines 21-45).**

3.9 As regards **Claim 10** the *Eisenhofer-1* reference discloses synchronizing different types of simulators **(Col. 11 Lines 60-67, Col. 12 Lines 1-25).**

3.10 As regards **Claims 13 and 15** the *Eisenhofer-1* reference discloses exchanging messages to enable simulators using different encoding schemes **(Col. 5 Lines 52-67, Col. 6 Lines 1-20, Col. 12 Lines 34-67, Col. 13 Lines 1-5).**

3.11 As regards **Claims 14, 16 and 17** the *Eisenhofer-1* reference discloses resolving conflicts based on boundary conditions between different simulators **(Figure 7, Col. 5 Lines 19-25, Col. 6 Lines 21-45, Col. 12 Lines 7-40).**

3.12 As regards **Claim 18** the *Eisenhofer-1* reference discloses high-level languages **(Col. 7 Lines 27-51).**

3.13 As regards **Claims 37 and 48** the *Eisenhofer-1* reference does not expressly discloses a message from a second device.

The *Worthington et al.* reference discloses getting a test message from a second device **(Figures 3, 4, 8, Col. 2 Lines 30-44).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have modified the *Eisenhofer-1* reference with the *Worthington et al.* reference because by providing entire multi-chip system models using individual system component models, an entire set of integrated circuits may be tested and simulated, not just individually, but in a manner that simulates how they will interact with each other such that problems in how the different chips interact can be detected before costly fabrication occurs ***(Worthington et al. Col. 1 Lines 45-51).***

4. **Claims 3, 7, 20, 23, 28, 33, 36, 44, 47,** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Eisenhofer et al. U.S. Patent 6,108,494** hereafter referred to as the *Eisenhofer–1* reference in view of **Worthington et al. U.S. Patent 5,881,270** and in further view of **Eisenhofer et al. U.S. Patent 6,339,836** hereafter referred to as the *Eisenhofer-2* reference and in further view of **Ly et al. U.S. Patent 6,175,946.**

4.1 As regards independent **Claims 1, 21, 26, 29, and 34** see the rejection in paragraph **3.1.**

4.2 As regards independent **Claims 40 and 45** see the rejection in paragraph **3.2.**

4.3 As regards **Claims 3, 20, 23, 28, 33, 36, 44, 47** the *Eisenhofer–1* reference does not expressly disclose a checker.

The *Ly et al.* reference discloses a checker **(Figure 1A, 5, 6, Col. 2 Lines 36-42).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention was made, to have modified the *Eisenhofer–1* reference with the *Ly et al.* reference because diagnosing errors flagged by automatically generated checkers is much easier than diagnosing errors flagged by end-to-end tests, ***(Ly et al. Col. 3 Lines 53-56).***

4.4 As regards **Claim 7** the *Eisenhofer–1* reference does not expressly disclose a tree.

The *Ly et al.* reference discloses a process control tree **(Figure 3A).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention was made, to have modified the *Eisenhofer–1* reference with the *Ly et al.* reference because diagnosing errors flagged by automatically generated checkers is much easier than diagnosing errors flagged by end-to-end tests, ***(Ly et al. Col. 3 Lines 53-56).***

5. **Claims 11 and 12** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Eisenhofer et al. U.S. Patent 6,108,494** hereafter referred to as the *Eisenhofer–1* reference in view of **Worthington et al. U.S. Patent 5,881,270** and in further view of **Eisenhofer et al. U.S. Patent 6,339,836** hereafter referred to as the *Eisenhofer-2* reference and in further view of **Dearth et al. U.S. Patent 5,881,267.**

5.1 As regards independent **Claim 1** see the rejection in paragraph **3.1.**

5.2 As regards **Claims 11 and 12** the *Eisenhofer–1* reference does not expressly disclose executing a remote procedure call.

The *Dearth et al.* reference discloses executing a remote procedure call **(Col. 10 Lines 45-56).**

It would have been obvious, at the time of the invention was made, to one of ordinary skill in the art to have modified the *Eisenhofer–1* reference with the *Dearth et al.* reference because the *Dearth et al.* reference discloses a method of improving the accuracy of a distributed simulation ***(Dearth et al. Col. 3 Lines 30-35).***

6. **Claim 19** is rejected under 35 U.S.C. 103(a) as being unpatentable over **Eisenhofer et al. U.S. Patent 6,108,494** hereafter referred to as the *Eisenhofer–1* reference in view of **Worthington et al. U.S. Patent 5,881,270** and in further view of **Eisenhofer et al. U.S. Patent 6,339,836** hereafter referred to as the *Eisenhofer-2* reference and in further view of **Dearth et al. U.S. Patent 5,732,247.**

6.1 As regards independent **Claim 1** see the rejection in paragraph **3.1** above.

6.2 As regards **Claim 19** the *Eisenhofer–1* reference does not expressly disclose handwritten test for all simulators.

6.3 The *Dearth et al.* reference discloses test written in a high-level language **(Figure 1).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention was made to have modified the *Eisenhofer–1* reference with the *Dearth et al.* reference because the *Dearth et al.* reference discloses an improved method to write test routines for hardware simulation ***(Dearth et al. Col. 2 Lines 14-20).***

7. **Claims 11 and 12** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Eisenhofer et al. U.S. Patent 6,108,494** hereafter referred to as the *Eisenhofer–1* reference in view of **Worthington et al. U.S. Patent 5,881,270** and in further view of **Eisenhofer et al. U.S. Patent 6,339,836** hereafter referred to as the *Eisenhofer-2* reference and in further view of **Dearth et al. U.S. Patent 5,732,247.**

7.1 As regards independent **Claim 1** see the rejection in paragraph **3.1.**

7.2 As regards **Claims 11 and 12** the *Eisenhofer–1* reference does not expressly disclose executing a remote procedure call.

The *Dearth et al.* reference discloses executing a remote procedure call that is deadlock safe **(Figures 4, 4A, 4B, 4C, 4D).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention was made to have modified the *Eisenhofer–1* reference with the *Dearth et al.* reference because the *Dearth et al.* reference discloses an improved method to write test routines for hardware simulation ***(Dearth et al. Col. 2 Lines 14-20).***

Conclusion

8. Claims 1-5 and 7-56 have been presented for reconsideration. The Claims have been reconsidered and rejected.

8.1 As a courtesy to the Applicant, the above action is made NON-FINAL to enable Applicant to respond without undue burden, wherein a First-Action Final Office Action would normally be appropriate (See MPEP 706.07(b)).

8.2 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwin M Craig whose telephone number is 703 305-7150. The examiner can normally be reached on 10:00 - 6:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703 305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DMC

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